Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	286	(microcontroller).ti.	USPAT	OR	OFF	2005/02/14 18:04
L2	6	1 and auto$8 with increment$20 with decrement$3	USPAT	OR	OFF	2005/02/14 18:10
L3	0	1 and auto$8 with increment$20 with decrement$3 with pointer	USPAT	OR	OFF	2005/02/14 18:06
L4	6	1 and auto$8 with (increment$20 adder$20) with (decrement$3 substract$5)	USPAT	OR	OFF	2005/02/14 18:10
L5	1287	712/228 712/229 712/248	USPAT	OR	OFF	2005/02/14 20:46
L6	0	5 and (automatic same increment$3 same decrement$3 same pointer$1 same microcontroller$1)	USPAT	OR	OFF	2005/02/14 20:47
L7	2	5 and (increment$3 same decrement$3 same pointer$1 same microcontroller$1)	USPAT	OR	OFF	2005/02/14 20:47
S1	49	("6032248" "5426769" "6076156")	USPAT	OR	OFF	2005/02/11 18:26
S2	3	("6032248" "5426769" "6076156").pn.	USPAT	OR	OFF	2005/02/11 17:29
S3	8	("6032248" "5426769" "6076156") and AID	USPAT	OR	OFF	2005/02/14 20:45
S4	0	automatic same increment$3 same decremnet$3 same pointer$1 same microcontroller$1	USPAT	OR	OFF	2005/02/11 18:43
S6	0	automatic same increment$3 same decrement$3 same pointer$1 same microcontroller$1	USPAT	OR	OFF	2005/02/11 18:43
S7	26	increment$3 same decrement$3 same pointer$1 same microcontroller$1	USPAT	OR	OFF	2005/02/11 18:43
S8	8	increment$3 same decrement$3 same pointer$1 same microcontroller$1 same data same (bit flag)	USPAT	OR	OFF	2005/02/14 18:04
S9	2	auto$6 same (increment$3 add$4) same (decrement$3 substract$4) same pointer$1 same microcontroller$1 same data same (bit flag)	USPAT	OR	OFF	2005/02/11 21:02

Terms used
8051 microcontroller pointer incrementing decrementing

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Relevance scale

1 Caches and Memory Systems: Storage allocation for embedded processors
Jan Sjödin, Carl von Platen
November 2001 **Proceedings of the 2001 international conference on Compilers, architecture, and synthesis for embedded systems**
Full text available: pdf(259.20 KB) Additional Information: full citation, abstract, references, citings, index terms

In an embedded system, it is common to have several memory areas with different properties, such as access time and size. An access to a specific memory area is usually restricted to certain native pointer types. Different pointer types vary in size and cost. For example, it is typically cheaper to use an 8-bit pointer than a 16-bit pointer. The problem is to allocate data and select pointer types in the most effective way. Frequently accessed variables should be allocated in fast memory, and fr ...

2 Compiling with code-size constraints
Mayur Naik, Jens Palsberg
February 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 1
Full text available: pdf(178.97 KB) Additional Information: full citation, abstract, references, index terms

Most compilers ignore the problems of limited code space in embedded systems. Designers of embedded software often have no better alternative than to manually reduce the size of the source code or even the compiled code. Besides being tedious and error prone, such optimization results in obfuscated code that is difficult to maintain and reuse. In this paper, we present a step towards code-size-aware compilation. We phrase register allocation and code generation as an integer linear programming p ...

Keywords: Banked architecture, integer linear programming, register allocation, space optimization

3 Code optimization techniques for embedded DSP microprocessors
Stan Liao, Srinivas Devadas, Kurt Keutzer, Steve Tjiang, Albert Wang
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**
Full text available: pdf(121.23 KB) Additional Information: full citation, references, citings, index terms

Keywords: code generation, digital signal processors, optimization

Terms used
microcontroller pointer incrementing decrementing bit automatically

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1 Caches and Memory Systems: Storage allocation for embedded processors
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November 2001 **Proceedings of the 2001 international conference on Compilers, architecture, and synthesis for embedded systems**
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2 An optimal memory allocation scheme for scratch-pad-based embedded systems
Oren Avissar, Rajeev Barua, Dave Stewart
November 2002 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 1 Issue 1
Full text available: pdf(396.62 KB) Additional Information: full citation, abstract, references, citings, index terms

This article presents a technique for the efficient compiler management of software-exposed heterogeneous memory. In many lower-end embedded chips, often used in microcontrollers and DSP processors, heterogeneous memory units such as scratch-pad SRAM, internal DRAM, external DRAM, and ROM are visible directly to the software, without automatic management by a hardware caching mechanism. Instead, the memory units are mapped to different portions of the address space. Caches are avoided due to the ...

Keywords: Memory, allocation, embedded, heterogeneous, storage

3 Implementation of a SDH STM-N IC for B-ISDN using VHDL based synthesis tools
Juan Carlos Calderón, Enric Corominas, José M. Tapia, Luis París
September 1994 **Proceedings of the conference on European design automation**
Full text available: pdf(612.55 KB) Additional Information: full citation, references, index terms

4 Caches and Memory Systems: Heterogeneous memory management for embedded

systems
Oren Avissar, Rajeev Barua, Dave Stewart
November 2001 **Proceedings of the 2001 international conference on Compilers, architecture, and synthesis for embedded systems**
Full text available: pdf(241.12 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a technique for the efficient compiler management of software-exposed heterogeneous memory. In many lower-end embedded chips, often used in micro-controllers and DSP processors, heterogeneous memory units such as scratch-pad SRAM, internal DRAM, external DRAM and ROM are visible directly to the software, without automatic management by a hardware caching mechanism. Instead the memory units are mapped to different portions of the address space. Caches are avoided because of th ...

Keywords: embedded, heterogeneous, memory, storage

5 Using the Alfa-1 simulated processor for educational purposes
Gabriel A. Wainer, Sergio Daicz, Luis F. De Simoni, Demian Wassermann
December 2001 **Journal on Educational Resources in Computing (JERIC)**, Volume 1 Issue 4
Full text available: pdf(238.65 KB) Additional Information: full citation, abstract, references, index terms

Alfa-1 is a simulated computer designed for computer organization courses. Alfa-1 and its accompanying toolkit allow students to acquire practical insights into developing hardware by extending existing components. The DEVS formalism is used to model individual components and to integrate them into a hierarchy that describes the detailed behavior of different levels of a computer's architecture. We introduce Alfa-1 and the toolkit, show how to extend existing components, and describe how ...

Keywords: DEVS formalism, modeling computer architectures, systems specification

6 Microcode development for microprogrammed processors
J. P-C Hwang, C. A. Papachristou, D. D. Cornett
December 1985 **ACM SIGMICRO Newsletter , Proceedings of the 18th annual workshop on Microprogramming**, Volume 16 Issue 4
Full text available: pdf(1.17 MB) Additional Information: full citation, abstract, references, citings, index terms

The aim of this paper is to develop a top-down design automation tool for digital system design such as microprogrammed processors. The package contains a hardware description language to specify the design, a microcode development module to generate an efficient microprogam for the microprogrammed processor's control, and a functional simulator module to verify the validity of the design. The goal of this project is to develop an interactive computer-aided design environment for specificat ...

7 Code optimization techniques for embedded DSP microprocessors
Stan Liao, Srinivas Devadas, Kurt Keutzer, Steve Tjiang, Albert Wang
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**
Full text available: pdf(121.23 KB) Additional Information: full citation, references, citings, index terms

Keywords: code generation, digital signal processors, optimization

8 The automated generation of cross-system software for supporting micro/mini computer systems

Gearold R. Johnson, Robert A. Mueller
March 1976 **ACM SIGPLAN Notices , Proceedings of the ACM SIGMINI/SIGPLAN interface meeting on Programming systems in the small processor environment**, Volume 11 Issue 4
Full text available: pdf(783.32 KB) Additional Information: full citation, abstract, references, index terms

ASM/GEN and SIM/GEN are a software system comprised of a set of independent FORTRAN program writer modules designed to generate micro computer and small minicomputer assemblers and simulators. It is simple enough to be used by those with limited architecture and programming backgrounds, but flexible and powerful enough to generate efficient and well-structured assemblers and simulators for small micro/mini computers with sophisticated architectures and instruction sets. This paper presents ...

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